REMARKS

Claims 1-5 are pending in the present application, with Claims 1 and 4 in independent form. Claims 1-5 were rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,243,447 (Bodenkamp et al.) in view of U.S. Patent No. 6,297,832 (Mizuyabu et al.). Bodenkamp et al. discloses an enhanced single frame buffer display system; and, Mizuyabu et al. discloses a method and apparatus for memory access scheduling in a video graphics system. The Examiner stated that Bodenkamp et al. disclosed all of the limitation of the claims except for a timing generator that allegedly is disclosed by Mizuyabu et al.

Bodenkamp et al. provides frame buffers for graphics and video data (see col. 5, lines 35-36). Bodenkamp et al. provides that YUV data is translated into RGB data (see col. 5, lines 46-47). Bodenkamp et al. provides a display controller to perform the compositioning functions for the graphics and video signals (see col. 6, lines 53-68).

Mizuyabu et al. provides a memory controller that receives data from a first and a second memory bank, sequences the data, schedules the data and outputs the data to a graphics display engine and a video display engine, which in turn supply outputs to a merging block (see FIG. 1 and its description).

Regarding Claims 1 and 4, an on-screen display (OSD) controller 26 includes a timing signal generator 22 and an OSD mixer 24. The timing signal generator generates a timing signal for alternately enabling the first memory 12 storing YUV data and second memory 20 storing RGB data for a write operation and a read operation, and applies the generated timing signal to the first and second memories. When the write operation is enabled by the timing signal of the timing signal generator, the OSD controller 26 stores the YUV data in the first memory. After that, when the read operation is enabled by the timing signal of the timing signal generator, the YUV data stored in the first memory 12 is converted to the RGB data through the display format converter 14 and the YUV-RGB converter 16 and the converted RGB data is read. Further, when the write operation is enabled by the timing signal of the timing signal generator, the OSD controller 26 stores the YUV data in the

second memory. After that, when the read operation is enabled by the timing signal of the timing signal generator, the converted RGB data stored in the second memory is read.

The converted RGB data read from the first memory and the RGB data from the second memory are input for mixing in an OSD mixer 24, and output as a color display data.

Bodenkamp et al. relates to an enhanced single frame buffer video display system. Bodenkamp et al. discloses at column 5, lines 6-13, 22-26, 35-38, 44-48, column 6, lines 52-64, column 7, lines 57-65, and in FIG. 1 that the graphics frame buffer 21 stores the RGB data, the video frame buffer 22 stores the YUV data, and the video DAC 27 converts the YUV data stored in the video frame buffer 22 in the RGB data. Moreover, referring to FIG.4 of Bodenkamp et al., the display controller 50 combines the graphic (YUV) data and video (RGB) data, and converts the data input from the display controller 50 into RGB data.

However, in FIG. 1, the RGB data is stored in the graphics frame buffer 21, the YUV data is stored in the video frame buffer 22, and the RGB data and the YUV data (converted into RGB data) are combined and output to the display unit. In order to use a single frame buffer instead of using the two frame buffers of Bodenkamp et al., Bodenkamp et al. discloses a display controller for converting the input data format type to the predetermined format type and outputting it to the single frame buffer. The display controller converts the input data to a predetermined format type, and outputs it to the single frame buffer. Bodenkamp et al. does not disclose an OSD controller combining RGB data, which is YUV data output from the first memory and converted, and RGB data of the second memory, and then outputting the combined data to the display unit.

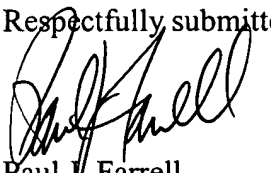
Furthermore, the two frame buffers (graphics frame buffer and video frame buffer) of Bodenkamp et al., respectively storing the corresponding data format (RGB data and YUV data), and the display controller converting the input data format type to the predetermined format type and outputting it to the single frame buffer for using a single frame buffer do not produce that which is recited in the claims of the present application.

Based on at least the foregoing, withdrawal of the rejection of Claims 1 and 4 is respectfully requested.

Independent Claims 1 and 4 are believed to be in condition for allowance. Without conceding the patentability per se of dependent Claims 2, 3 and 5, these are likewise believed to be allowable by virtue of their dependence on their respective amended independent claims. Accordingly, reconsideration and withdrawal of the rejections of dependent Claims 2, 3 and 5 is respectfully requested.

Accordingly, all of the claims pending in the Application, namely, Claims 1-5, are believed to be in condition for allowance. Should the Examiner believe that a telephone conference or personal interview would facilitate resolution of any remaining matters, the Examiner may contact Applicant's attorney at the number given below.

Respectfully submitted,



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